LEE – 10/743,454
Client/Matter: 021906-0307405

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for planarizing a surface of a semiconductor wafer, comprising:

depositing an insulator layer on the semiconductor wafer;

performing a first polishing process on a surface of the insulator layer deposited on the semiconductor wafer while supplying slurry to the surface of the insulator layer to polish about 80% thickness of a total polishing target of the insulator layer; and

performing a second polishing process on the surface of the insulator layer while supplying water to the surface of the insulator layer to polish the remainder of the insulator layer.

wherein the insulator layer is an inter metal dielectric layer made of fluorinated silicate glass ("FSG"), undoped silicate glass ("USG"), tetraethoxysilicate ("TEOS") or SiH.

2. (Cancelled).

3. (Cancelled).

4. (Cancelled).